INTRODUCTION

You hit the power button on your television and it instantly comes to life. But do the same thing with your computer and you have to wait a few minutes while it goes through its boot up sequence. Why can't we have a computer that turns on as instantly as a television or radio? IBM, in cooperation with Infineon, is promising to launch a new technology in the next few years that will eliminate the boot-up process. Magnetic random access memory (MRAM) has the potential to store more data, access that data faster and use less power than current memory technologies. The key to MRAM is that, as its name suggests, it uses magnetism rather than electrical power to store data. This is a major leap from **dynamic RAM** (DRAM), the most common type of memory in use today, which requires a continuous supply of electricity and is terribly inefficient. Twenty-five years ago, DRAM overtook ferrite core memory in the race to rule the PC memory market. Now it looks like ferromagnetic technology could be making a comeback, with IBM Corp. and Infineon Technologies charging a joint team of 80 engineers and scientists with the task of making magnetic RAM (MRAM) a commercial reality within four years

ATTRACTIONS OF THIS NEW TECHNOLOGY

Consider what happens when power goes off while you are typing on your computer? Unless you are connected to an uninterruptible power supply you lose everything you were working on since you last saved the document. That's because your computer's random access memory (RAM), which stores information for fast access, can't function without power. The same goes for your cellphone and PDA. Both require a battery to keep the RAM intact with your phone numbers and personal data. But IBM researchers have developed a new form of RAM — magnetic RAM (MRAM) — that doesn't forget anything when the power goes out.

MRAM promises to be

- Cheap
- Fast
- Nonvolatile
- Low power alternative

MRAM has these attractions over conventional RAM, which uses electrical cells to store data, as MRAM uses magnetic cells. This method is similar to the way your hard drive stores information. When you remove power from your computer, conventional RAM loses memory, but the data on your hard disk remains intact due to its magnetic orientation, which represents binary information. Because magnetic

memory cells maintain their state even when power is removed, MRAM possesses a distinct advantage over electrical .

With DRAM (RAM used in PCs and workstations) you store a charge in a capacitor.That charge will leak away over time and it needs to be refreshed frequently that takes power. But with MRAM you have no such problems .You need no power to maintain the state,and toy only need to pass a small current through the memory to read it.

Compared with SRAM(RAM used to build fast memory,cache) MRAMs are as fast as SRAM with read/write speeds better than 2.5 nanoseconds.Moreover MRAMs can be build smaller than SRAM and hence would be cheaper.

Compared to Flash memory(an example for Flash memory is computer's BIOS chip), its much faster to write on to MRAM.Thus MRAM threatens to replace not only dynamic RAM, but also Flash memory. (Flash memory is used for easy and fast information storage in such devices as digital cameras and home video game consoles. In fact, Flash memory is considered a **solid state** storage device. Solid state means that there are no moving parts -- everything is electronic instead of mechanical.)

HOW MRAM WORKS

INSTANT ON COMPUTING

When you turn your computer on, you can hear it revving up. It takes a few minutes before you can actually get to programs to run. If you just want to browse the Internet, you have to wait for your computer's start-up sequence to finish before you can go to your favorite Web sites. You push the computer's power button, there's some beeping and humming, you see flashes of text on the screen and you count the seconds ticking by. It's a very slow process. Why can't it simply turn on like your television? -- hit a button and instantly your Internet browser is ready to go. What is it that your computer has to do when you turn it on .

Every computer has a basic input/output system (BIOS) that performs a series of functions during the boot up sequence. The series of functions performed by BIOS includes

- A power-on self-test (POST) for all of the different hardware components in the system to make sure everything is working properly
- Activating other BIOS chips on different cards installed in the computer - For example, SCSI and graphics card often have their own BIOS chips
- Providing a set of low level routines that the operating system uses to interface different hardware devices
- Manage a collection of settings for the hard disks,clock etc

The BIOS is a type of software that your computer needs to function properly. It is usually stored on a Flash Memory chip on the motherboard, but sometimes the chip is another type of ROM. Its most important function is to load the computer's operating system when you

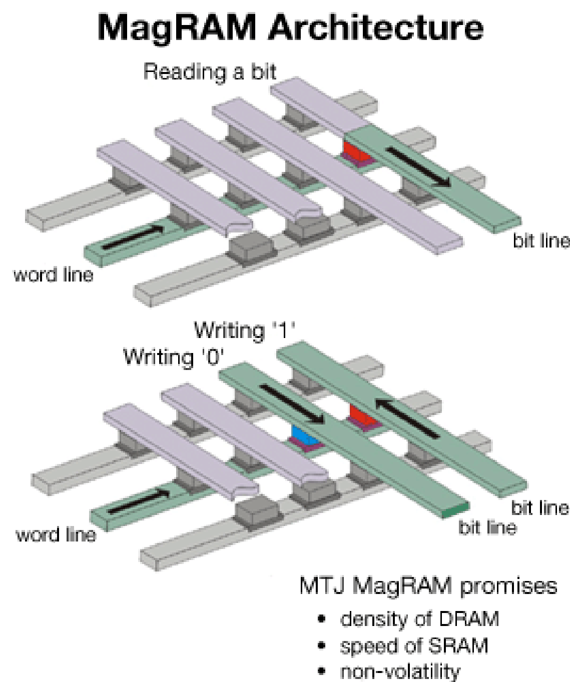
turn the computer on. During a cold boot(The start-up of a computer from a powered-down state), the BIOS also checks the RAM by performing a read/write test of each memory address. The first thing the BIOS does is check the information stored in a tiny amount of RAM (64 bytes) located on a **complementary metal oxide semiconductor** (CMOS) chip**.**

MRAM would eliminate the tedium of boot-up because it would use magnetism, rather than electricity, to store bits of data. MRAM will slowly begin to replace DRAM starting sometime in 2003. DRAM wastes a lot of electricity because it needs to be supplied with a constant current to store bits of data. In a DRAM configuration, a capacitor operates like a small bucket storing electrons. To store a 1 in a memory cell, the bucket is filled with electrons. To store a 0, the bucket is emptied. DRAM has to be refreshed thousands of times per second to retain a 1.

MAGNETIC RAM ARCHITECTURE

Like Flash memory, MRAM is a nonvolatile memory -- a **solid-state chip** that has no moving parts. Unlike with DRAM chips, you don't have to continuously refresh the data on solid-state chips. Flash memory can't be used for instant-on PCs because it hasn't demonstrated long-term reliability. MRAM will likely compete with Flash memory in the portable device market for the same reason that it will replace DRAM -- it reduces power consumption.

In MRAM only a small amount of electricity is needed to store bits of data. This small amount of electricity switches the polarity of each memory cell on the chip. A memory cell is created when **wordlines** (rows) and **bitlines** (columns) on a chip intersect. Each one of these cells stores a 1 or a 0, representing a piece of data. MRAM promises to combine the high speed of static RAM (SRAM), the storage capacity of DRAM and the non-volatility of Flash Memory.



Here's how MRAM works. Two small magnetic layers separated by a thin insulating layer make up each memory cell, forming a tiny magnetic "sandwich." Each magnetic layer behaves like a tiny bar magnet, with a north pole and south pole, called a magnetic "moment." The moments of

the two magnetic layers can be aligned either parallel (north poles pointing in the same direction) or antiparallel (north poles pointing in opposite directions) to each other. These two states correspond to the binary states — the 1s and 0s — of the memory. The memory writing process aligns the magnetic moments, while the memory reading process detects the alignment. With MRAM, bits are stored in thin magnetic layers in the direction of magnetization.

READING DATA

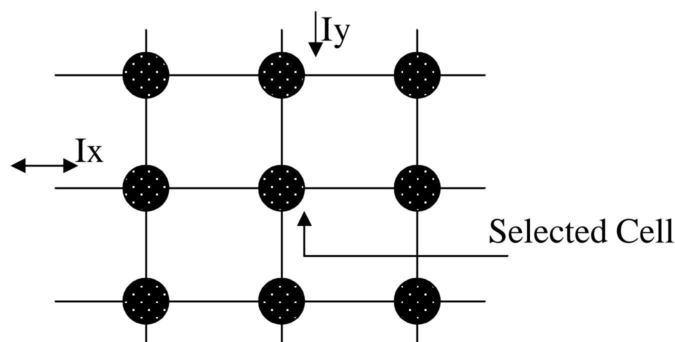
To read the bit of information stored in this memory cell, you must determine the orientation of the two magnetic moments. Passing a small electric current directly through the memory cell accomplishes this. When the moments are parallel, the resistance of the memory cell is smaller than when the moments are not parallel. Even though there is an insulating layer between the magnetic layers, the insulating layer is so thin that electrons can "tunnel" through it from one magnetic layer to the other.

WRITING DATA

To write to the device, you pass currents through wires close to (but not connected to) the magnetic cells. Because any current through a wire generates a magnetic field, you can use this field to change the direction of the magnetic moment. The arrangement of the wires and cells is called a cross-point architecture: the magnetic junctions are set up along the

intersection points of a grid. Wires — called word lines — run in parallel below the magnetic cells. Another set of wires — called bit lines — runs above the magnetic cells and perpendicular to the set of wires below. Like coordinates on a map, choosing one particular word line and one particular bit line uniquely specifies one of the memory cells. To write to a particular cell (bit), a current is passed through the two independent wires (one above and one below) that intersect at that particular cell. Only the cell at the crosspoint of the two wires sees the magnetic fields from both currents and changes state.

MRAM works by etching a grid of criss-crossing wires on a chip in two layers—with the horizontal wires being placed just below the vertical wires. At each intersection, a “magnetic tunnel junction” (MTJ) is created that serves as a switch—and thus as a repository for a single bit of memory. The MTJ is essentially a small magnet whose direction is easily flipped. Common materials for the MTJ include chromium dioxide and iron-cobalt alloys. Current runs perpendicularly, "tunneling" through the insulator that separates it from a sheath of copper. At the base of one of the electrodes is a fixed anti-ferromagnetic layer that creates a strong coupling field**.** When a magnetic field is applied, electrons flow from one electrode to another, creating 0 and 1 states.



2-D Magnetic Memory Cell Array

DEVELOPING MRAM

BACKGROUND

The development of MRAM has been based on a number of significant ideas ,over the past 20 years starting with Cross-tie Random Access Memory (CRAM), and then using higher sensitive giant magnetoresistance (GMR) and Spin Dependent Tunneling (SDT) materials. A brief background on precursors to magnetoresistive random access memory (MRAM) and then descriptions of cell configurations with improved signal levels including MRAM cells with GMR materials,cells using SDT structures

Early magnetic random access memory (as opposed to serial memories like tape and disk) used the natural hysteresis of magnetic materials to store data (‘1”or “0”) by using two or more current carrying wires or straps. Magnetic elements were arrayed so that only ones which were to be written received a combination of magnetic fields above a write threshold, while the other elements in the array did not change storage state. Most of today’s MRAM concepts still use this write technique.

These early memories (mostly magnetic core memories) used inductive

signals for determining the storage state (“1” or “0”). A magnetic field (current) was used to “interrogate” the memory element, and the polarity of induced voltages in a sensing circuit depended on whether a “1” or “0” was stored.The first to propose a magneto-resistive readout scheme was Jack Raffel. His scheme stored data in a magnetic body, which in turn produced a stray magnetic field that could be detected by a separate magnetoresistive sensing element. The concept was not high density because it was difficult to get a sufficiently large external stray field from a small magnetic storage cell. This scheme of separating the magnetic storage element from the sensor has similarity with the schemes recently proposed for magnetized bodies sensed by Hall effect sensors

The first technology which used a magnetic element for storage and also used the same element for magnetoresistance readout was the Cross-tie Cell Random Access Memory (CRAM). This cell used a slight difference in resistance of the cell depending on the presence or absence of a Block point to indicate a “1” or “0” . There were difficulties in getting the cell to write consistently, and the difference in resistance between a “1” and “0” was only about 0.1% of the inherent cell resistance, an impractically low signal.

MAGNETIC TUNNEL JUNCTIONS

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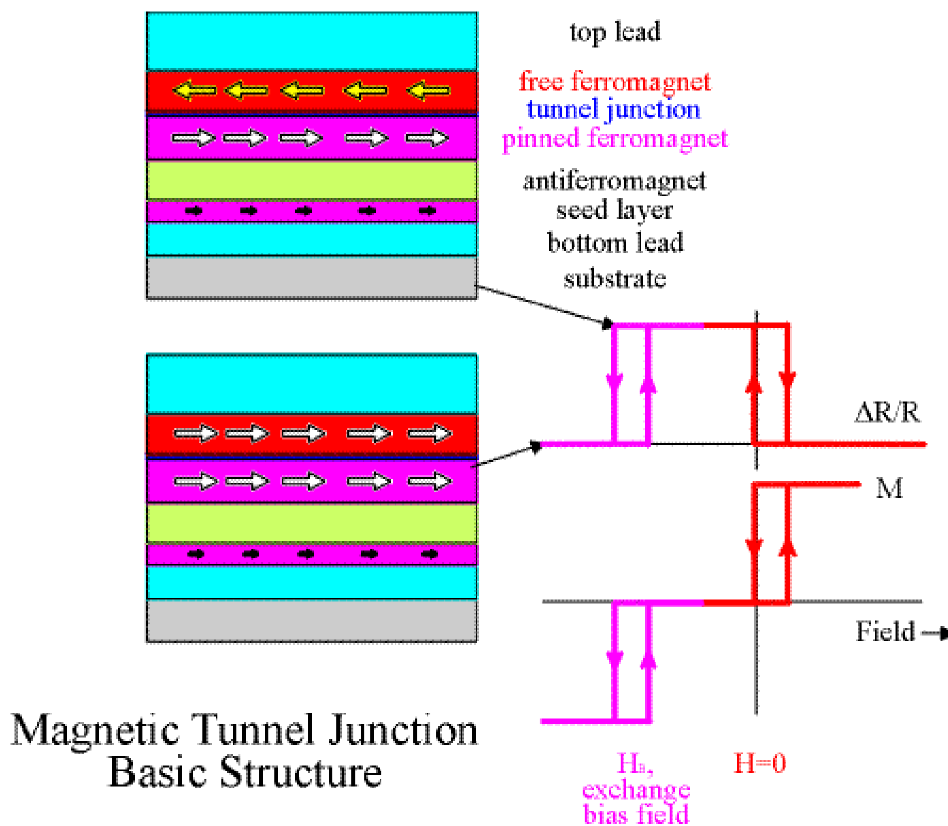
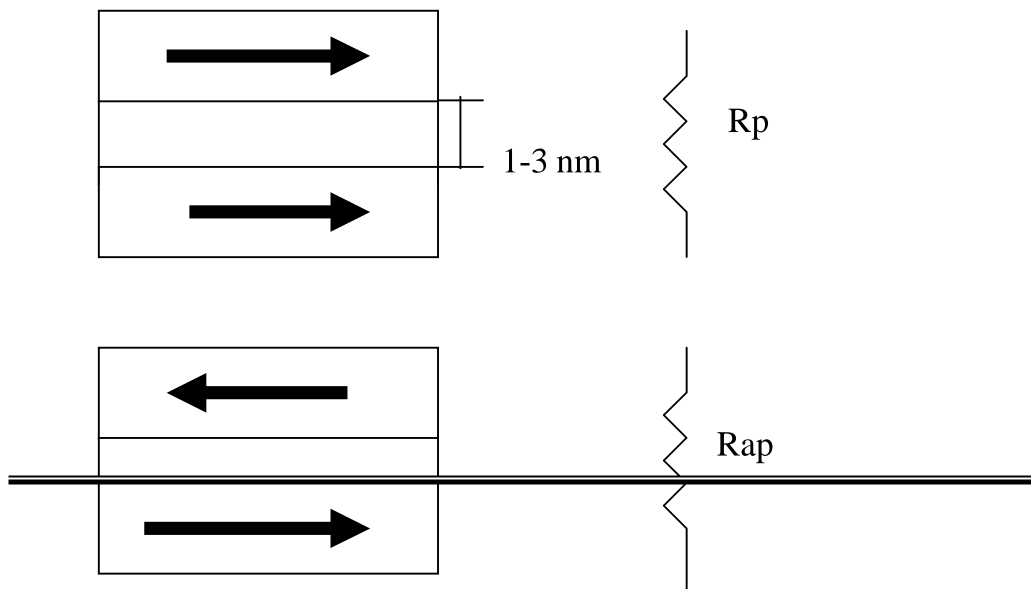


Hence tunneling current between two metallic magnetic layers separated by a very thin insulating barrier (magnetic tunnel junction, MTJ)

depends on the relative orientation of the magnetization in the adjacent magnetic layers.

Little progress has been made until the mid-nineties and by now it is possible to fabricate ferromagnet-insulator-ferromagnet tunnel junctions with magnetoresistance effects of 20% and more at room temperature.. The high magnetoresistance at room temperature and generally low magnetic switching fields makes these junctions promising candidates for the use as magnetic sensors and non-volatile memory elements for a next generation of (high density) information handling. In view of these technological applications, the magnetic tunnel junctions intrinsically possess a number of characteristic features, such as:

- the intrinsic high resistivity and low power consumption
- the high D*R*/*R*
- small dimensions allowing high densities
- expected thermal robustness
- radiation resistant
- intrinsically fast response.



The above figure shows a schematic representation of a magnetic tunnel junction: two metallic ferromagnetic electrodes separated by an insulator. The **parallel** and **antiparallel** magnetic configurations of the electrodes have different resistance. The switching between both states by application of a magnetic field brings about a magnetoresistive effect which can be used in several technological applications. Rp and Rap is the resistance of the tunnel junction in the parallel and antiparallel configurations respectively. Between the parallel and antiparallel magnetic configurations, magnetoresistance ratios as large as 50%.

Large magnetoresistance ratios ratios at room temperature (~20-30%) were recently reported in tunnel junctions composed of transition metal ferromagnets (Fe, Co, Ni) as electrodes and alumina (Al_2O_3) barriers. Their growth and patterning is rather well controlled and they could constitute the core of the first-generation magnetic-tunnel-junctions-based devices.

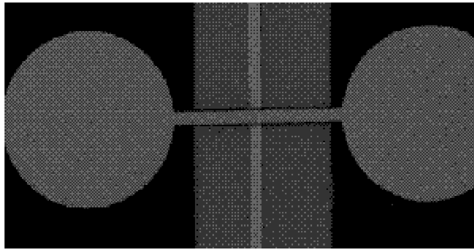
The **parallel** and **antiparallel** magnetic configurations of the electrodes spin of the electron, which is an intrinsic microscopicmagnet carried by each electron.The electrons keep their spin direction and the probability

of tunnelling from the first electrode for one electron with a certain spin direction depends on the number of states with the same spin direction available in the second electrode .Thus,it is not equivalent for the tunnelling electrons the parallel and antiparallel configurations because they correspond to different densities of states of the electrodes and, consequently, to different resistances.

The **spin polarisation** is a subtle concept related to the difference between the number of spin-up and –down electrons participating in a certain electronic process. In this definition spin-up electrons means electrons with spin parallel to the magnetisation and spin-down electrons, antiparallel to the magnetisation. Therefore, a positive spin polarisation means that there are more electrons with spin parallel to the magnetisation and a negative spin polarisation means the contrary.

Much of the research has focused on engineering these ferromagnetic materials to have the other needed properties:

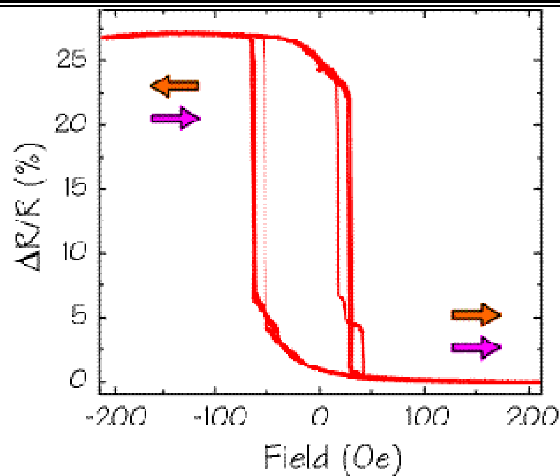
- Ability to rotate the magnetic moments using a very small magnetic field
- A smaller overall resistance
- An increased resistance differential between the two states — up from 10 percent to 50 percent. This differential makes distinguishing the two states of memory simple and reliable: you pass a small current through the device and monitor the voltage drop.



Scanning electron microscope image of
typical metal-masked magnetic tunnel junction,
80 µm x 80 µm in area.

Junctions were directly fabricated using computer-controlled placement of up to 8 different metal shadow masks. The masks can be successively placed on any one of up to twenty 1 inch diameter wafers with a placement accuracy of ~±40 µm. By using different masks, between 10 to 74 junctions of size ~80x80μm^2 can be fashioned on each wafer. An optical micrograph of a typical junction is shown in this MJT picture. The tunnel barrier is formed by oxidation of a thin Al layer deposited at ambient temperature. In order to manipulate the relative orientation of the magnetic moments of the two electrodes in a more controlled fashion we have developed magnetic tunnel junction structures in which one of the magnetic layers is exchange biased using an antiferromagnetic layer**.**

Magnitude of the magnetoresistance would largely be dependent on the interface between the tunnel barrier and the magnetic electrodes



Typical resistance versus field loop of a lithographically patterned magnetic tunnel junction, 2x4µm^2 in area.

GIANT MAGNETORESISTANCE

Metallic multilayers comprised of alternating ferromagnetic and non-ferromagnetic spacer layers, each a few atomic layers thick, display fascinating properties. These properties arise from quantum confinement of electrons in spin-dependent potential wells provided by the ferromagnet/spacer layer boundaries. In a ferromagnetic metal there exists two current channels, one that can conduct a current better than the other. Thus the fascinating properties arise from quantum confinement of electrons in spin-dependent potential wells provided by the ferromagnet/spacer layer boundaries. An important observation is that ferromagnet transition metals are indirectly magnetically exchange coupled via spacer layers comprised of almost any of the non-ferromagnetic transition metals. The magnetic coupling of the spacer layer and its strength varies systematically with the spacer d-band filling.

The period of the coupling is related to the detailed electronic structure of the spacer metal and can, for example, be tuned by varying the composition of the spacer layer, or by varying its crystallographic orientation.

The resistance of metallic multilayered structures depends on the magnetic arrangement of the magnetic moments of the individual magnetic layers, leading to oscillations in resistance in zero field with spacer layer thickness and large variations in resistance with magnetic field. This latter phenomenon has been called "Giant Magnetoresistance (GMR)". GMR has captured much attention since GMR multilayers display much larger magnetoresistance (MR) than any simple metal or alloy at room temperature.

The origin of GMR derives from spin-dependent scattering of the conduction carriers within the magnetic layers or at the boundaries of the magnetic layers. Experiments show convincingly the predominance of spin-dependent scattering at the ferromagnet/spacer layer interfaces. For example, subtle modifications of the interfaces, by insertion of sub-monolayer equivalents of additional magnetic material, can give rise to drastic changes in magnetoresistance . These changes depend on the magnetic and electronic character of the modifed interface, so that the magnetoresistance itself becomes a valuable probe of the interface.

With GMR, the current flows horizontally rather than perpendicularly and does not use an insulator layer. We have seen in TMR technology, MRAMs sandwich a layer of insulating material between two electrodes of magnetic material, such as ion nickel. Current runs perpendicularly,

"tunneling" through the insulator that separates it from a sheath of copper. At the base of one of the electrodes is a fixed anti-ferromagnetic layer that creates a strong coupling field. When a magnetic field is applied, electrons flow from one electrode to another, creating 0 and 1 states

GMR technology has a much lower magnetic resistance (MR) ratio than TMR. GMR's ratio is about 7 percent and has the potential to increase to about 15 percent. That limits is potential performance compared with TMR, which has the potential to hit 30 percent to 40 percent. Thus GMR technology, many researchers say GMR is not viable for commercial applications. Rather, tunneling magnetic resistance (TMR) is expected to be the basis of future MRAM.

ADVANCED MRAM CONCEPTS

Two important goals of Magnetoresistive Random Access Memory (MRAM) development are to improve MRAM manufacturability and to extend MRAM density to 100 nm dimensions. One potential barrier to MRAM manufacturability is associated with the method of write selection in which two orthogonal currents in coincidence must write data, whereas each of the orthogonal currents alone cannot disturb the data. This "2D" selection method places constraints on uniformity of MRAM Memory cells. Using a transistor per cell for write select greatly improves operating margins and lowers write currents. In this new scheme, a select transistor per memory cell is used for writing, and a much smaller current is used for reading than for writing. This should result in substantially wider process margins, but probably at the

sacrifice of density due to the size of the required transistor in the cell. This "1D magnetic select" scheme is potentially ideal for small, high performance nonvolatile RAM.

A technique to increase density of MRAM by heating an antiferromagnetic pinning layer above its ordering temperature (Neel temperature). This deepens the energy well depth of unselected cells, and potentially will permit higher storage densities at smaller current levels.

1D MAGNETIC SELECTION

Selected cells receive both Ix and Iy currents, and are switched into the desired memory states. The currents must be selected so that Iy or Ix separately do not disturb the memory state of stored data. Bits on the same x line or y line that are not being written are subjected to "half-select" currents which tend to disturb the data. If very large currents are used to insure the writing of worst case cells, then the half-select currents are also large and tend to disturb the most disturb-sensitive cells.

The half-selected memory states are also not nearly as stable as stored and they provide the majority of projected cell failures in time. In addition to half-select currents, these cells must withstand stray fields from neighboring cells and fields from leakage currents and stray environmental fields. Thus, the requirements for uniformity and design margins present challenges in manufacturing the 2D magnetic arrays.

Most magnetoresistive memory schemes also use a 2D selection scheme for reading data. The original MRAM concept use magnetic 2D selection

schemes for reading, which introduce further disturb conditions. Magnetic tunnel junction memories (MTJ) use a diode or transistor to select a memory cell for reading, and thus do not have significant disturb conditions for reading, but they still have the constraints of 2D magnetic selection for writing.

"1D selection" scheme for both reading and writing a magnetoresistive memory cell improves reliability. A high current of either polarity (plus current for a "1" and negative current for a "0") is passed through a select transistor and through the memory cell to write. A lower current is used to generate a voltage across the cell which will be higher or lower depending on the data stored and the magnetoresistance of the cell. This voltage is then sensed and compared to a reference in order to determine the memory state.
Note that the transistor provides the selection of the memory cell, not the 2D magnetic switching properties of the cell. A very large current can be used to write and a small current can be used to read the cell, thus providing potentially very large margins. Of course it is important to use as small a current as will reliably write the cell so as to reduce the size of the transistor needed for selection.There are still 2D arrays of cells, but the transistors take up the burden of selection rather than placing severe constraints on the magnetic switching properties of the cell. This is why this is called a "1D magnetic selection". The scheme is quite similar to that used for DRAM where a transistor is used to write and detect charge on a capacitor.

NEEL POINT WRITTEN CELLS

Another challenge for very high density MRAM is cell stability at nm dimensions. As the cell size shrinks and the volume, V, of magnetic materials gets smaller, thermal agitation can cause a cell to lose data. (This same problem gives rise to the so called " superparamagnetic limit" spoken of in recording technology"). If Ht is the switching threshold of a half-selected cell and Ms is the magnetic moment, then the depth of the energy well associated with that switching threshold in the half-select state is proportional to Ms*Ht*V. For low error rates the ratio of this energy well depth to kT should be at least 55. Assuming a maximum operating temperature of 350 K and a cell size of 100nm X 100nm X 2 (nm), one finds that Ht ie the switching threshold of a half-selected cell, must be several times that of the threshold of a non-half-selected cell. When enough current is applied to get this magnitude of field in a nm sized cell, thermal heating is a problem, and kT becomes even larger, and the higher densities are even harder to achieve.

An approach to improving the density of MRAM is to make use of heating effects in combination with magnetic fields from currents to switch cells which use antiferromagnetic pinning of a ferromagnetic layer.The process of pinning includes two magnetic films sandwich a conducting layer, and one of the two magnetic films is "pinned" with an antiferromagnet across a stripe etched from the materials. A magnetic field created by a current through the stripe can be used to magnetize the unpinned magnetic film in either of two directions, depending on the direction of the current. Then a smaller current through the stripe can be used to sense the value of resistance –higher if the films are oppositely magnetized and lower if they are magnetized in the same direction. A large current can be used for writing without disturbing other cells, and a

much lower current can be used for sensing. This would suggest large margins. After pinning, very large magnetic fields (several thousands of Oe) cannot permanently reverse the pinned direction if the temperature is significantly below the Neel (ordering) temperature of the antiferromagnet. This property could be used in many memory cells to obtain a deep energy well for stored data, and provided heat can be applied to the cell for writing, the writing currents may not have to be very large.

These were approaches for making a producible, high performance memory and approaches for extending the density of MRAM to nm dimensions. It should be noted that these techniques could be used in combination. There are undoubtedly many more possibilities for improving MRAM density, performance, and producibility that will come to light in the next few years.

CURRENT STATUS

Magnetic RAM is not an overnight technological feat. It has taken nearly three decades to develop. To give you an idea of when IBM began working on MRAM, Microsoft didn't even exist when IBM made its first breakthrough in this technology. In 1974, IBM Research developed a miniature computer component called the magnetic tunnel junction. This component was eventually used to store information.

The potential market for MRAM is big. It is expected to eventually become the memory standard for future electronics, replacing DRAM. In

The potential market for MRAM is big. It is expected to eventually become the memory standard for future electronics, replacing DRAM. In MRAM has the potential to replace today's memory technologies in electronic products of the future," said Bijan Davari, IBM Vice President of Technology and Emerging Products. He added that the announcement of MRAM's impending availability is a major step in moving the technology from the research stage to product development.

By 2003, IBM and Infineon expect to have test chips in use. Initial chips will only be able to accommodate 256 megabytes of data. There are already some removable Flash Memory that can hold that much data. However, IBM researchers believe that they could increase the data-storage size by the time it reaches volume production in 2004. MRAM then will be made available to consumers in limited quantities.

It will probably take atleast a decade before we see MRAM chips become a mainstream storage medium. By then, who knows what we will be looking at? Holographic memory(CDs, DVDs and magnetic storage all store bits of information on the surface of a recording medium. In order to increase storage capabilities, scientists are now working on a new optical storage method, called **holographic memory**, that will go beneath the surface and use the volume of the recording medium for storage, instead of only the surface area.) is projected to be available as early as 2003. It will be able to store 125 gigabytes and produce transfer rates of about 40 megabytes per second. The

combination of MRAM and holographic memory, both being developed by IBM, could result in a desktop computer than can hold tons of data, work faster and use less power than its most high-tech predecessors.

Because MRAM is non-volatile, there is never a need to flush data to disk every time your system off .It also improves file system data bandwidth by freeing disk from the need to handle frequent metadata accesses.

IBM researcher Stuart Parkin used this sputtering machine to create magnetic tunnel junctions, a key to MRAM technology

CHALLENGES FACED

While progress has been made in determining the structure and materials needed for MRAM development, there are still many hurdles to jump before MRAM chips can be made production-worthy. Among the issues to tackle are architectures, materials development, submicron manufacturing, wiring, and the feasibility of integrating MRAM with logic.

Present day challenges for MRAM technology include

- Reducing drive currents
- Eliminating cell instabilities due to magnetization vortices
- Improving modes of operation at nanometer dimensions fundamental thermal instabilities
- Finding applications with sufficient volumes and performance advantages to make MRAM manufacturing costs competitive

To be practical, dense MRAM cells should operate with less than a few mA currents when the lithography is at the 0.2 – 0.3 micron dimensions. Two reasons are: to stay within the current carrying capability of thin, narrow metal lines, and to be compatible with the center-to-center circuit spacing at the edge of the magnetic array. Reported data shows more than 10 times the desired current densities. Several mitigating ideas have emerged. One is to coat or "keeper" the tops and edges of the strip lines used in the memory array. This is done to reduce word currents by a factor of 3. An additional idea is to reduce the rise time of pulses, which takes advantage of the gyro-magnetic nature of the magnetization. This technique has reduced the required drive currents by a factor of more than 2. Devising methods whereby required current levels scale down with size of the memory cell will continue to be a challenge for MRAM.

In the 1980's it was believed that as the memory cells approached the dimensions of a domain wall width, there would be no more problems with multi-domain magnetization in the cells, i.e. the magnetization would act as a single collection of spins with only one rest state. This myth was shown to be false by both experiment and data. Anomolies called "vortices" can occur in cells as small as a few tenths of a micron in diameter. This can be prevented but at the expense of cell

area. Recently, a circumferential magnetization storage mode in round MRAM cells has been proposed. Vortices are the unanticipated problem in MRAM technology.

The stability of the MRAM cell can be looked at as an energy well problem,where the energy associated with storage is MHcV, where Hc is a critical field which prevents magnetization reversal, M is the saturation magnetization, and V is the volume of the magnetic material in the cell. As the volume is reduced, the ratio approaches some multiple of kT (about 20) at which the error rate in the memory becomes unacceptable. Making Hc ever higher does not work because of the current required to write and the resultant heating of the cell (raising kT). With the present modes of operating, the practical lower limit to MRAM storage area would be about 0.1 micron on a side. A new idea is to use heat to help select the cell for writing and use the Curie point of an antiferromagnet to enable writing with a low current. Then at cooler temperatures, the energy well can be very deep.

We used photo- and electron-beam lithography to create working MTJ memory cells on a silicon substrate. This is an essential first step for many aspects of our research. We are continuing to develop processes that will provide uniformly high-quality structures across the entire working surface. It is critical that all the MTJs operate with nearly identical characteristics.

We reduced the MTJ device resistance more than 10-million-fold. Because the overall resistance of a magnetic tunnel junction increases as

the junction dimensions decrease, MTJs must have a proportionally lower resistance as the feature size decreases in order to make practical high-density chips. By carefully controlling the thickness and integrity of the aluminum dioxide tunnel barrier (no pinholes can be tolerated!), the resistance has been reduced from 1 billion ohm-microns-squared to 60 ohm-microns-squared. The barrier, which is as thin as 10 angstroms -- about four atomic layers -- is created by depositing and then oxidizing a thin film of aluminum.

We increased the low-field TMR five-fold: from 10 percent to nearly 50 percent. MJTs with increased TMR produce a larger signal, which has many practical benefits, including permitting more flexibility in designing circuits. Two factors led to the increased TMR: a) Optimizing the ferromagnetic cobalt-iron alloy, and b) designing MTJs with the same sort of "anti-ferromagnetic biasing" that makes GMR heads for disk drives so successful.

We measured MTJ reading and writing times as fast as 10 nanoseconds -- some six times faster than today's fastest DRAM memory. Such an extremely fast speed results from both the high TMR and low device resistance.

We have increased the thermal stability of MTJ structures from 100 C to about 250 C. We expect to need further testing and improvements in thermal stability before we can use MTJs in applications.

The last challenge is getting MRAM into high production levels. It requires investment, and a lot of it, perhaps as much as a billion dollars.

It will take commitment from one or more companies to manufacture RAM in high volume, in order to realize the tremendous potential of MRAM as a mainstream nonvolatile me mory technology, but with the right investment, MRAM can be a very important mainstream memory technology.

ANTICIPATED APPLICATIONS

MRAM combines many of the advantages of presently available forms of memory. IBM researchers have demonstrated that MRAM can be six times faster than the industry standard's dynamic RAM (DRAM), and it is almost as fast as today's static RAM (SRAM) — a faster, more expensive RAM used in memory caches. MRAM also has the potential to be. extremely dense, packing more information into a smaller space. The 1,000-bit prototype is significantly denser than conventional static RAM.

The most important attribute of MRAM is its nonvolatility. In the absence of any electrical power, the magnetic moments maintain their alignment. Thus, the data is kept intact. This feature could enable instant-on computers, because the memory state would be maintained when you turned your computer off.

This instant-on ability doesn't just apply to desktop computers. "The most likely application for MRAM will be in pervasive computing devices," Parkin says. As portable wireless devices become universal, devices such as PDAs and cell phones will require the dense, fast, relatively inexpensive nonvolatile memory that MRAM can provide.

In the United States, a research program in magnetic materials and devices was launched in '94, sharing the costs with Honeywell, IBM, and Motorola. Several other U.S. companies have developed products based on GMR technology, and last winter, Hewlett-Packard said it intends to join IBM and Motorola in the TMR market.The anticipated applications of this collective effort is funding spin-electronics research in hopes of exploiting nonvolatile-memory capabilities in embedded systems for use in satellites, strategic missiles, avionics, and other mission-critical applications. For instance, coding information for satellites could be loaded on rad-hard MRAM devices that would ensure satellites remain on station.

Rebooting aircraft computers using traditional storage technologies delays operations on the flight line. Nonvolatile MRAM technology "would change the way the military operates", researchers believe .

Beyond military applications, government researchers envision MRAM technology showing up within five years in embedded applications, such as cell phones and digital cameras. The dawn of the MRAM-based laptop, which will eliminate boot-up delays, will take longer, scientists say.

“The payoff is going to be in all the mobile applications," the Naval Research Laboratory's Prinz said, particularly when gigabit MRAM chips can be integrated into cell phones to dump data onto hard drives.

HP, meanwhile, will pit its MRAMs against more-expensive flash memories. HP also plans to combine MRAMs with atomic-resolution storage technology to replace hard drives. Mike Matson, general manager of HP's Information Storage Group, said he expects the combined technology to grab half the traditional hard-drive market over time.

Parallel disk storage can have significant benefits to enabling warfighting capabilities. Military applications, including ballistic missile controls and multi-theater troop management, afford considerable challenges for rapid data storage and retrieval. Health applications, particularly biomedical research, often require similar high density, rapid access disk storage capabilities that could benefit from advances in this technology

CONCLUSION

If MRAM chips are to debut ,the completely different architecture will make DRAM chips obselete and issue a new era of memory chips.

MRAM solves your problem of losing data typed on your computer unless you are connected to uninterruptible power supply ,as MRAM doesn't forget anything when power goes out. The difference is conventional RAM, uses electrical CELLS to store data, MRAM uses magnetic cells. This method is similar to the way your hard drive stores information. When you remove power from your computer, conventional RAM loses memory, but the data on your hard disk remains intact due to its magnetic orientation, which represents binary information. Because magnetic memory cells maintain their state even when power is removed, MRAM possesses a distinct advantage over electrical cells.

There is still a long way to go before MRAM is ready for prime time. Neither IBM nor Motorola, for instance, is expected to go into mass production until they prove that they can make 256 megabit chips—the standard memory module used today. But, as total sales of computer memory in 2000 were estimated by Semico Research Corporation to have been worth $48 billion, manufacturers have a considerable incentive to ensure that MRAM becomes a serious challenger for DRAM's crown.

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ABSTRACT

Magnetic RAM (MRAM) is a new memory technology with access and cost characteristics comparable to those of conventional dynamic RAM (DRAM) and the non-volatility of magnetic media such as disk. That is MRAM retains its memory even after removing power from the device. Such a non-volatile memory has important military applications for missiles and satellites. Clearly such a device could also have important commercial applications if the non-volatility were accomplished without impacting other properties of the memory, notably density, read and write speed, and lifetime. IBM in cooperation with Infineon is promising to launch this new technology ,that will eliminate the boot-up process of a computer and thus enable it to turn on as instantly as a television or radio, using memory cells based on magnetic tunnel junctions.

This paper discusses the following aspects in detail:

- Attractions of this new technology
- How MRAM works
- MRAM Architecture
- Magnetic Tunnel Junctions – future of MRAM
- Challenges faced
- Anticipated Applications

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