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INTRODUCTION

We are now living in a world driven by various electronic equipments. Semiconductors form the fundamental building blocks of the modern electronic world providing the brains and the memory of products all around us from washing machines to super computers. Semi conductors consist of array of transistors with each transistor being a simple switch between electrical 0 and 1. Now often bundled together in there 10's of millions they form highly complex, intelligent, reliable semiconductor chips, which are small and cheap enough for proliferation into products all around us.

Identification of new materials has been, and still is, the primary means in the development of next generation semiconductors. For the past 30 years, relentless scaling of CMOS IC technology to smaller dimensions has enabled the continual introduction of complex microelectronics system functions. However, this trend is not likely to continue indefinitely beyond the semiconductor technology roadmap. As silicon technology approaches its material limit, and as we reach the end of the roadmap, an understanding of emerging research devices will be of foremost importance in the identification of new materials to address the corresponding technological requirements.

If scaling is to continue to and below the 65nm node, alternatives to CMOS designs will be needed to provide a path to device scaling beyond the end of the roadmap. However, these emerging research technologies will be faced with an uphill technology challenge. For digital applications, these challenges

include exponentially increasing the leakage current (gate, channel, and source/drain junctions), short channel effects, etc. while for analogue or RF applications, among the challenges are sustained linearity, low noise figure, power added efficiency and transistor matching. One of the fundamental approaches to manage this challenge is using new materials to build the next generation transistors.

PRESENT MEMORY TECHNOLOGY SCENARIO

As stated, revising the memory technology fields ruled by silicon technology is of great importance. Digital Memory is and has been a close comrade of each and every technical advancement in Information Technology. The current memory technologies have a lot of limitations. DRAM is volatile and difficult to integrate. RAM is high cost and volatile. Flash has slower writes and lesser number of write/erase cycles compared to others. These memory technologies when needed to expand will allow expansion only two-dimensional space. Hence area required will be increased. They will not allow stacking of one memory chip over the other. Also the storage capacities are not enough to fulfill the exponentially increasing need. Hence industry is searching for “Holy Grail” future memory technologies that are efficient to provide a good solution. Next generation memories are trying tradeoffs between size and cost. These make them good possibilities for development.

EMERGING MEMORY TECHNOLOGIES

Many new memory technologies were introduced when it is understood that semiconductor memory technology has to be

replaced, or updated by its successor since scaling with semiconductor memory reached its material limit. These memory technologies are referred as 'Next Generation Memories". Next Generation Memories satisfy all of the good attributes of memory. The most important one among them is their ability to support expansion in three-dimensional spaces. Intel, the biggest maker of computer processors, is also the largest maker of flash-memory chips is trying to combine the processing features and space requirements feature and several next generation memories are being studied in this perspective. They include MRAM, FeRAM, Polymer Memory Ovonic Unified Memory, ETOX-4BPC, NRAM etc. One or two of them will become the mainstream.

FUNDAMENTAL IDEAS OF EMERGING MEMORIES

The fundamental idea of all these technologies is the bistable nature possible for of the selected material. FeRAM works on the basis of the bistable nature of the centre atom of selected crystalline material. A voltage is applied upon the crystal, which in turn polarizes the internal dipoles up or down. I.e. actually the difference between these states is the difference in conductivity. Non –Linear FeRAM read capacitor, i.e., the crystal unit placed in between two electrodes will remain in the direction polarized (state) by the applied electric field until another field capable of polarizing the crystal's central atom to another state is applied.

In the case of Polymer memory data stored by changing the polarization of the polymer between metal lines (electrodes). To activate this cell structure, a voltage is applied between the top and bottom electrodes, modifying the organic material. Different voltage polarities are used to write and read the cells. Application of an

electric field to a cell lowers the polymer's resistance, thus increasing its ability to conduct current; the polymer maintains its state until a field of opposite polarity is applied to raise its resistance back to its original level. The different conductivity States represent bits of information.

In the case of NROM memory ONO stacks are used to store charges at specific locations. This requires a charge pump for producing the charges required for writing into the memory cell. Here charge is stored at the ON junctions.

Phase change memory also called Ovonic unified memory (OUM), is based on rapid reversible phase change effect in materials under the influence of electric current pulses. The OUM uses the reversible structural phase-change in thin-film material (e.g., chalcogenides) as the data storage mechanism. The small volume of active media acts as a programmable resistor between a high and low resistance with > 40X dynamic range. Ones and zeros are represented by crystalline versus amorphous phase states of active material. Phase states are programmed by the application of a current pulse through a
MOSFET, which drives the memory cell into a high or low resistance state, depending on current magnitude. Measuring resistance changes in the cell performs the function of reading data. OUM cells can be programmed to intermediate resistance values; e.g., for multistate data storage.

MRAMs are based on the magnetoresistive effects in magnetic materials and structures that exhibit a resistance change when an external magnetic field is applied. In the MRAM, data are stored by applying magnetic fields that cause magnetic materials to be magnetized into one of two possible magnetic states. Measuring

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resistance changes in the cell compared to a reference performs reading data. Passing currents nearby or through the magnetic structure creates the magnetic fields applied to each cell.

OVONIC UNIFIED MEMORY

Among the above-mentioned non-volatile Memories, Ovonic Unified Memory is the most promising one. “Ovonic Unified Memory” is the registered name for the non-volatile memory based on the material called chalcogenide.

The term “chalcogen” refers to the Group VI elements of the periodic table. “Chalcogenide” refers to alloys containing at least one of these elements such as the alloy of germanium, antimony, and tellurium discussed here. Energy Conversion Devices, Inc. has used this particular alloy to develop a phase-change memory technology used in commercially available rewriteable CD and DVD disks. This phase change technology uses a thermally activated, rapid, reversible change in the structure of the alloy to store data. Since the binary information is represented by two different phases of the material it is inherently non-volatile, requiring no energy to keep the material in either of its two stable structural states.

The two structural states of the chalcogenide alloy, as shown in Figure 1, are an amorphous state and a polycrystalline state. Relative to the amorphous state, the polycrystalline state shows a dramatic increase in free electron density, similar to a metal. This difference in free electron density gives rise to a difference in reflectivity and resistivity. In the case of the re-writeable CD and DVD disk technology, a laser is used to heat the material to change states. Directing a low-power laser at the material and detecting the

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difference in reflectivity between the two phases read the state of the memory.

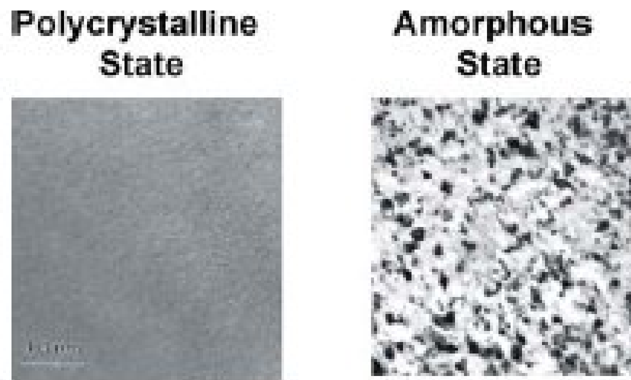

FIGURE 1

Ovonyx, Inc., under license from Energy Conversion Devices, Inc., is working with several commercial partners to develop a solid-state nonvolatile memory technology using the chalcogenide phase change material. To implement a memory the device is incorporated as a two terminal resistor element with standard CMOS processing. Resistive heating is used to change the phase of the chalcogenide material. Depending upon the temperature profile applied, the material is either melted by taking it above the melting temperature (T_m) to form the amorphous state, or crystallized by holding it at a lower temperature (T_x) for a slightly longer period of time, as shown in Figure 2. The time needed to program either state is = 400ns. Multiple resistance states between these two extremes have been demonstrated, enabling multi-bit storage per memory cell. However, current development activities are focused on single-bit applications. Once programmed, the memory state of the cell is determined by reading its resistance.

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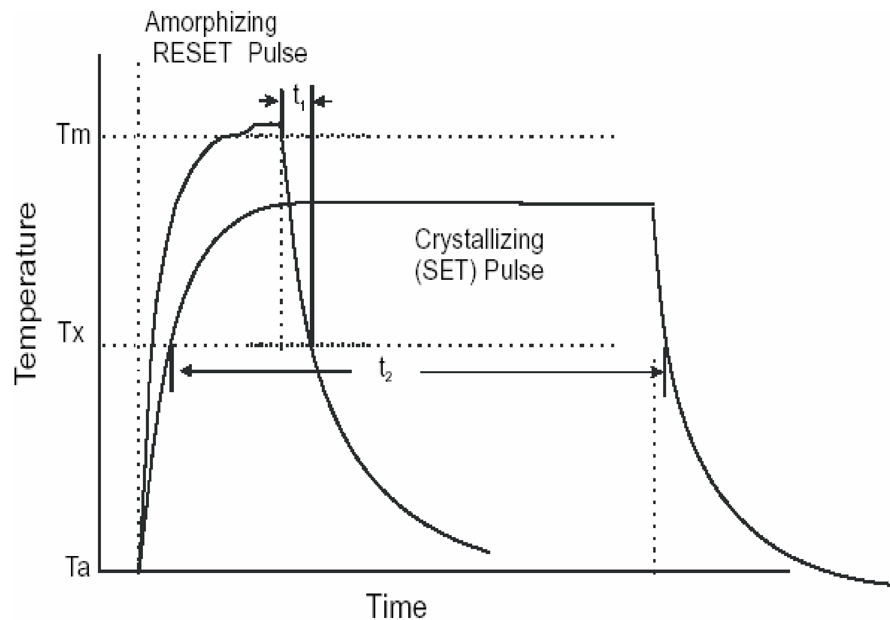


FIGURE 2

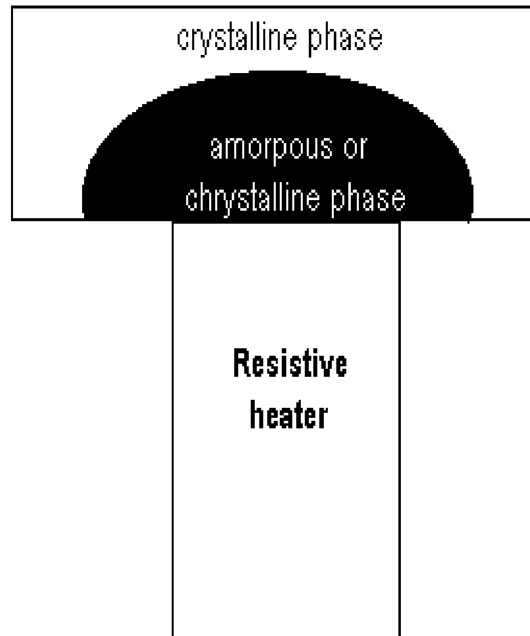
Since the data in a chalcogenide memory element is stored as a structural phase rather than an electrical charge or state, it is expected to be impervious to ionizing radiation effects. This inherent radiation tolerance of the chalcogenide material and demonstrated write speeds more than 1000 times faster than commercially available nonvolatile memories make it attractive for space based applications. A radiation hardened semiconductor technology incorporating chalcogenide based memory elements will address both critical and enabling space system needs, including standalone memory modules and embedded cores for microprocessors and ASICs. Previously, BAE SYSTEMS and Ovonyx have reported on the results of discrete memory elements fabricated in BAE SYSTEMS' Manassas, Virginia facility. These devices were manufactured using standard semiconductor process equipment to sputter and etch the chalcogenide material. While built in the same line used to fabricate

radiation-hardened CMOS products, these memory elements were not yet integrated with transistors. They were discrete two-terminal programmable resistors, requiring approximately 0.6 mA to set the device into a low resistance state, and 1.3 mA to reset it to the high resistance state. One billion (1E9) write cycles between these two states were demonstrated. Reading the state of the device is non-destructive and has no impact on device wear out (unlimited read cycles).

OUM ATTRIBUTES

- Non volatile in nature
- High density ensures large storage of data within a small area
- Non destructive read:-ensures that the data is not corrupted during a read cycle.
- Uses very low voltage and power from a single source.
- Write/erase cycles of 10e12 are demonstrated
- Poly crystalline
- This technology offers the potential of easy addition of non volatile memory to a standard CMOS process.
- This is a highly scalable memory
- Low cost implementation is expected.

OUM ARCHITECTURE



A memory cell consists of a top electrode, a layer of the chalcogenide, and a resistive heating element. The base of the heater is connected to a diode. As with MRAM, reading the micrometer-sized cell is done by measuring its resistance. But unlike MRAM the resistance change is very large-more than a factor of 100. Thermal insulators are also attached to the memory structure in order to avoid data lose due to destruction of material at high temperatures.

To write data into the cell, the chalcogenide is heated past its melting point and then rapidly cooled to make it amorphous. To make it crystalline, it is heated to just below its melting point and held there for approximately 50ns, giving the atoms time to position themselves in their crystal locations.

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INTEGRATION WITH CMOS

Under contract to the Space Vehicles Directorate of the Air Force Research Laboratory (AFRL), BAE SYSTEMS and Ovonyx began the current program in August of 2001 to integrate the chalcogenide-based memory element into a radiation-hardened CMOS process. The initial goal of this effort was to develop the processes necessary to connect the memory element to CMOS transistors and metal wiring, without degrading the operation of either the memory elements or the transistors. It also was desired to maximize the potential memory density of the technology by placing the memory element directly above the transistors and below the first level of metal as shown in a simplified diagram in Figure 3.

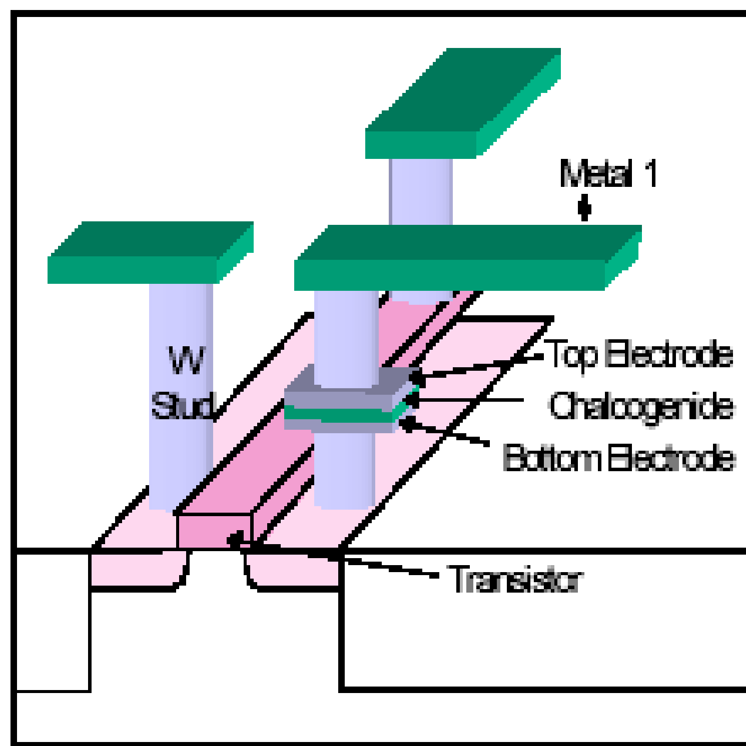

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FIGURE 3

To accomplish this process integration task, it was necessary to design a test chip with appropriate structures. This vehicle was called the Access Device Test Chip (ADTC) since each memory cell requires an access device (transistor) in addition to the chalcogenide memory element. Such a memory cell, comprised of one access transistor and one chalcogenide resistor, is herein referred to as a 1T1R cell. The ADTC included 272 macros, each with 2 columns of 10 probe pads. Of these, 163 macros were borrowed from existing BAE SYSTEMS' test structures and used to verify normal transistor operation. There were 109 new macros designed to address the memory element features. These included sheet resistance and contact resistance measurement structures, discrete memory elements of various sizes and configurations, and two 16-bit 1T1R memory arrays.

Short loop (partial flow) experiments were processed using subsets of the full ADTC mask set. These experiments were used to optimize the process steps used to connect the bottom electrode of the memory element to underlying tungsten studs and to connect an additional tungsten stud level between Metal 1 and the top electrode of the memory element. A full flow experiment was then processed to demonstrate integrated transistors and memory elements.

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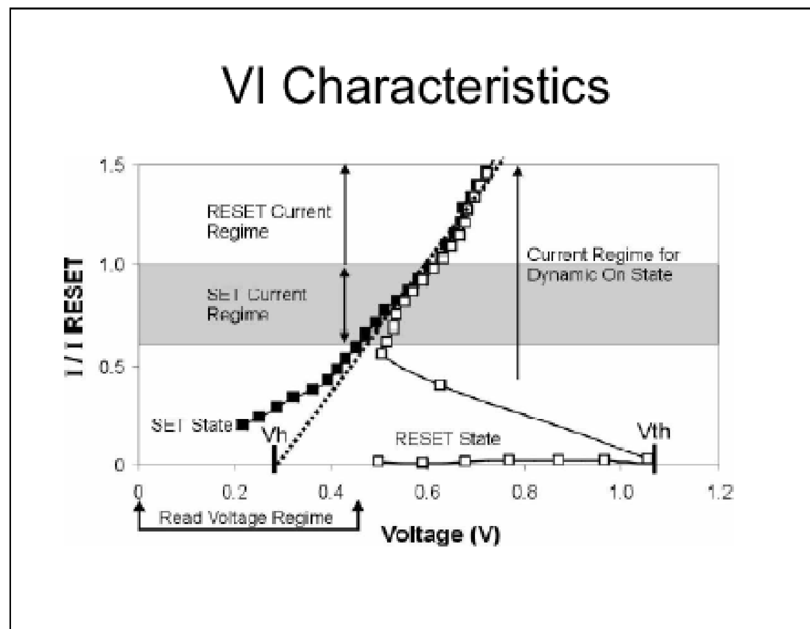

FIGURE 4

Figure 4 shows the I-V characteristic for a 1T1R memory cell successfully fabricated using the ADTC vehicle. The voltage is applied to one of the two terminals of the chalcogenide resistor, and the access transistor (biased on) is between the other resistor terminal and ground. The high resistance amorphous material shows very little current below a threshold voltage (VT) of 1.2V. In this same region the low resistance polycrystalline material shows a significantly higher current. The state of the memory cell is read using the difference in I-V characteristics below VT. Above VT, both materials display identical I-V characteristics, with a dynamic resistance (RDYNAMIC) of ˜1k. In itself, this transition to a low resistance electrical state does not change the structural phase of the material. However, it does allow for heating of the material to program it to the low resistance state (1) or the high resistance state (0). Extrapolation of the portion of the I-V curve that is above VT to the X-axis yields a point referred to as a holding voltage (VH). The

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applied voltage must be reduced below VH to exit the programming mode.

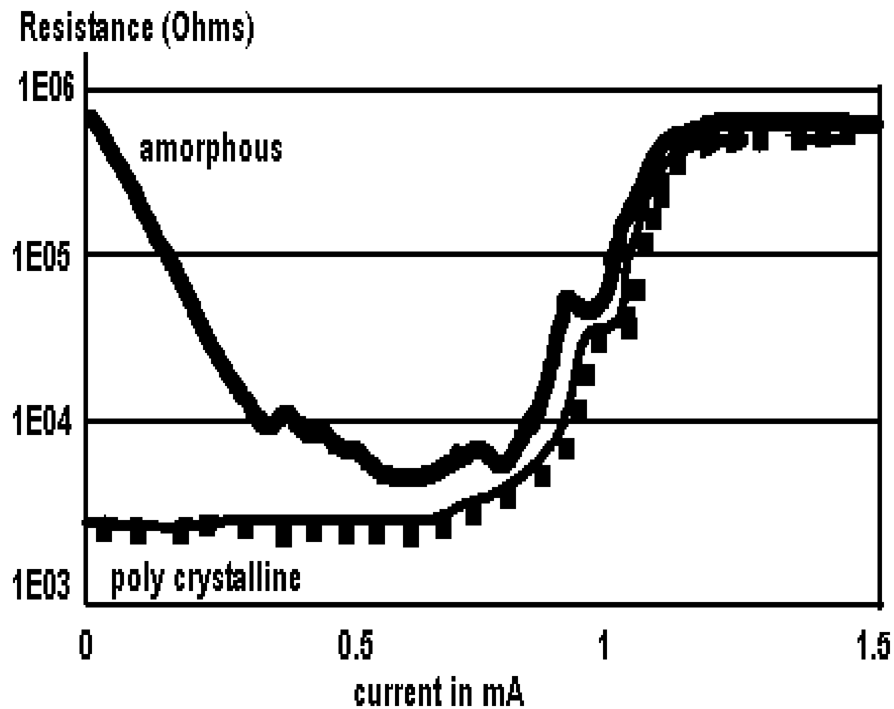

FIGURE 5

Figure 5 shows the operation of a 1T1R memory, again with the access transistor biased on. The plotted resistance values were measured below V_T, while the current used to program these resistances were measured above V_T. Similar to the previously demonstrated stand-alone memory elements, these devices require approximately 0.6 mA to set to the low resistance state (R_{SET}) and 1.2 mA to reset to the high resistance state (R_{RESET}). The circuit was verified to be electrically open with the access transistor biased off.

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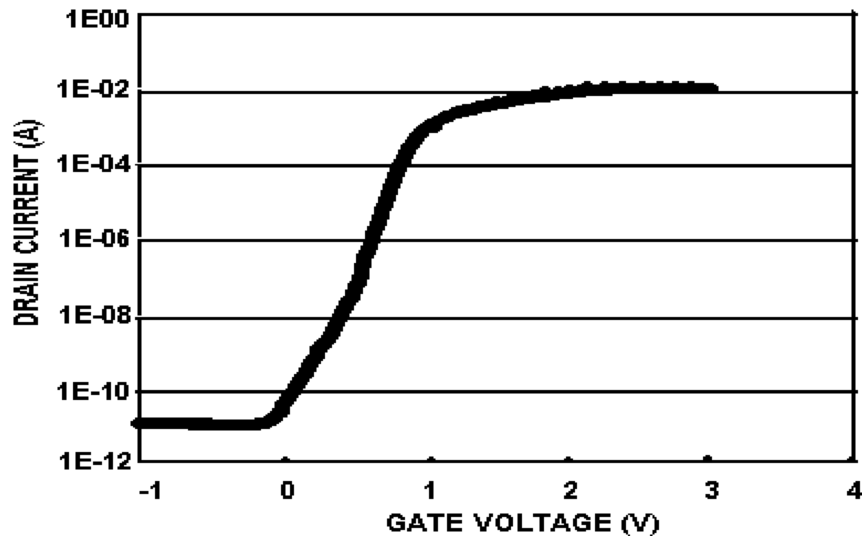

FIGURE 6

Figure 6 shows the total dose (X-ray) response of N-channel transistors processed through the chalcogenide memory flow. The small threshold voltage shift is typical of BAE SYSTEMS' standard radiation-hardened transistor processing. All other measured parameters (drive current, threshold voltage, electrical channel length, contact resistance, etc.) were also typical of product manufactured without the memory element.

CIRCUIT DEMONSTRATION

In order to test the behavior of chalcogenide cells as circuit elements, the Chalcogenide Technology Characterization Vehicle (CTCV) was developed. The CTCV contains a variety of memory arrays with different architecture, circuit, and layout variations. Key goals in the design of the CTCV were: 1) to make the read and write circuits robust with respect to potential variations in cell electrical characteristics; 2) to test the effect of the memory cell

layout on performance; and 3) to maximize the amount of useful data obtained that could later be used for product design. The CTCV was sub-divided into four chiplets, each containing variations of 1T1R cell memory arrays and various standalone sub circuits. Standalone copies of the array sub circuits were included in each chiplet for process monitoring and read/write current experiments.

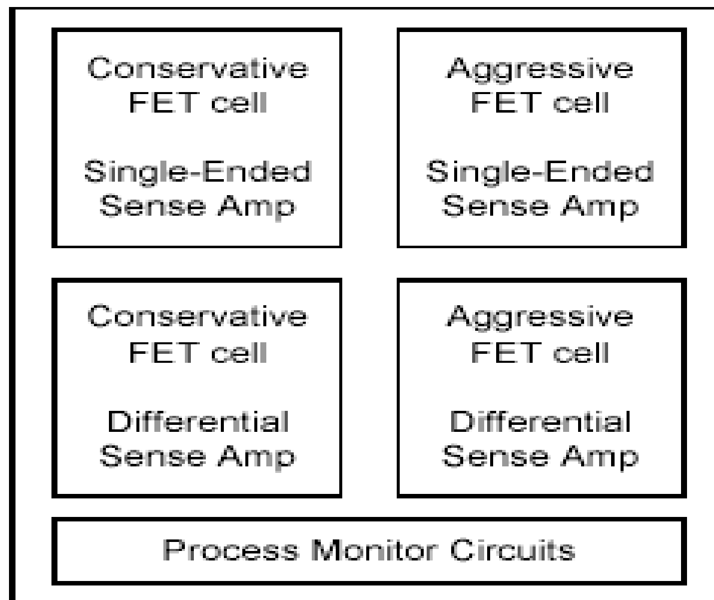

FIGURE 7

A diagram of one of the chiplets is shown in Figure 7. The arrays all contain 64k 1T1R cells, arranged as 256 rows by 256 columns. This is large enough to make meaningful analyses of parasitic capacitance effects, while still permitting four variations of the array to be placed on each chiplet. The primary differences between arrays consist of the type of sense amp (single-ended or differential) and variations in the location and number of contacts in the memory cell.

The data in the single-ended arrays is formatted as 4096 16-bit words (64k bits), and in the differential arrays as 4096 8-bit words (32k bits). The 256 columns are divided into 16 groups of 16. One sense amplifier services each group, and the 16 columns in each group are selected one at a time based on the four most significant address bits. In simulations, stray capacitance was predicted to cause excessive read settling time when more than 16 columns were connected to a sense amp. Each column has its own write current river, which also performs the column select function for write operations.

The single-ended sense amplifier reads the current drawn by a single cell when a voltage is applied to it. The differential amplifier measures the currents in two selected cells that have previously been written with complementary data, and senses the difference in current between them. This cuts the available memory size in half, but increases noise margin and sensitivity. In both the single-ended and differential sense amplifiers, a voltage limiting circuit prevents the chalcogenide element voltage from exceeding V_T, so that the cell is not inadvertently re-programmed.

On one chiplet, there are two arrays designed without sense amplifiers. Instead, the selected column outputs are routed directly to the 16 I/O pins where the data outputs would normally be connected. This enables direct analog measurements to be made on a selected cell. A third array on this chiplet has both the column select switches and the sense amplifiers deleted. Eight of the 256 columns are brought out to I/O pins. This enables further analog measurements to be made, without an intervening column select transistor.

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"Conservative" and "aggressive" layout versions of the chalcogenide cell were made. The conservative cell is larger, and has four contacts to bring current through to the bottom and top electrodes of the memory cell. The aggressive cell contains only two contacts per electrode, reducing its size. The pitch of the larger cell was used to establish row and column spacing in all arrays. The aggressive cell could thus be easily substituted for the conservative cell. Short wires were added to the smaller cell to map its connection points to those of the larger. This permitted testing both cells in one array layout without requiring significant additional layout labor.

A final variation in the cell design involved contact spacing. The contacts on the bottom electrode were moved to be either closer to or farther away from the chalcogenide "pore." This allows assessment of the effect of contact spacing on the thermal and electrical characteristics of the chalcogenide pore.

Process monitoring structures were included on each chiplet to aid in calibration of memory array test data. These consist of a standalone replica of each of the Write and Read (single-ended) circuits, a CMOS inverter, and a 1T1R cell. The outputs of each of these circuits were brought out to permit measurement of currents versus bias voltages.

Pins were provided on the CTCV for external bias voltage inputs to vary the read and write current levels. The standalone copies of the read/write circuits are provided with all key nodes brought out to pins. These replica circuits permit the read and write currents to be programmed by varying the bias voltages. This allows

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more in-depth characterization to be performed in advance of designing a product. In an actual product, on-chip reference circuits would generate bias voltages. In the write circuit, a PFET driver is connected to each column, and is normally turned off by setting its gate bias to V_{DD}. When a write is to occur, the selected driver's gate is switched to one of two external bias voltages for the required write pulse time. The bias voltages can be calibrated to set the write drive currents to the levels needed to reliably write a one or a zero. The data inputs determine which bias voltage is applied to each write driver.

For the read circuit, several cell resistance-sensing schemes were investigated during CTCV development. The adopted scheme applies a controlled voltage to the cell to be read, and the resulting current is measured. Care is taken not to exceed V_T during a read cycle. The sense amplifier reflects the read current into a programmable NFET load, thus generating a high (1) or low (0) output. The gate bias of all sense amplifier loads can be varied in parallel to change the current level at which the output voltage switches. The bias levels are calibrated via a standalone copy of the read circuit that has all key nodes brought out to pins. The NFET load's output is buffered by a string of CMOS inverters to provide full CMOS logic voltage swing, and then routed to the correct data output I/O pad driver.

When a read circuit supplies a current to a selected cell, the cell's corresponding column charges up toward the steady state read voltage. The column voltage waveform is affected by the programmed resistance and internal capacitances of each of the cells in the column, and thus is pattern dependent. The combined charge from all of the column's cells during this charging process may travel into

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the sense amplifier input, momentarily causing it to experience a transient, which could prevent the accessed cells' data from being read correctly. To minimize this effect, each column is discharged after a write, and recharged before a read.

Transistor parametric and discrete memory element test structures were tested on the CTCV lot at the wafer level. These tests served two purposes. The first goal was to confirm that the extra processing steps involved in inserting the chalcogenide flow had no effect on the base CMOS technology. No statistical differences in transistor parametric values were noted between these wafers and standard 0.5µm RHCMOS product.

The second goal of wafer test was to measure the set, reset and dynamic programming resistances (R_{SET}, R_{RESET} and $R_{DYNAMIC}$), threshold and holding voltages (V_T and V_H), and required programming currents (I_{SET} and I_{RESET}) of stand-alone, two terminal chalcogenide memory elements. These values were used to set the operating points of the write driver circuits and the bias point of the sense amp.

To allow debug of the CTCV module test setup in parallel with the wafer test effort, one wafer was selected and diced to remove the CTCV die. Five die of one of the four chiplets, (chip 1) were sent ahead through the packaging process. Chip 1 has four different array configurations, two 64 kbit, single ended sense amp arrays and two 32 kbit, differential sense amp arrays. Two of the arrays were constructed with the conservative cell layout and two with the aggressive cell layout. Functional test patterns used on these send-ahead devices included all zeros, all ones, checkerboard and checkerboard bar. The results of this testing showed that all circuit

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functional blocks (control circuits, addressing, data I/O, write 0/1, and sense amp) performed as designed. All four of the array configurations present on the chip showed functional memory elements, i.e., memory cells could be programmed to zero or one and subsequently read out. As more packaged parts become available, more exhaustive test patterns will be employed for full characterization.

The five send-ahead devices were also used for determining the optimum bias points of the three externally adjustable parameters: write 0 drive current, write 1 drive current, and the sense amp switching point. An Integrated Measurements Systems XTS-Blazer tester was used to provide stimulus and measure response curves. A wide range of load conditions was chosen based on the measurements performed at wafer test.

A family of drive current vs. bias voltage curves was constructed for both on-chip programming drive circuits across various values of $R_{DYNAMIC}$. These curves validate design simulations and demonstrate adequate operating range of each of the circuits.

Likewise, a family of switching point curves was generated at various R_{SET} and R_{RESET} values using the standalone sense amp built onto each die. These curves were used to determine the optimal sense amp DC bias point for the test chips and demonstrated the ability of the sense amp to distinguish the 0 and 1 state within the range of chalcogenide resistance values measured at wafer test.

TEST RESULTS

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Test results confirmed that the insertion of a chalcogenide manufacturing flow had no effect on measured CMOS transistor parametric and did not change the total dose response of the base technology. Preliminary results on send-ahead packaged parts indicate full functionality of the 64 kbit memory arrays. Further characterization of the ADTC wafers and packaged devices from the CTCV wafers will include chalcogenide material-specific studies, such as write cycle endurance (a.k.a. "cycle life"), operating and storage temperature effects and further radiation effects tests on packaged parts, to include total dose (60Co) and heavy ion exposure. Minimum write and read cycle timing, layout spacing evaluation, data pattern insensitivity and other design related characterization will be conducted to support product optimization.

Companies working with Ovonic Unified memory have their ultimate goal to gather enough data to begin a product design targeting a 1–4 Mbit C-RAM device that is latch-up and SEU immune to greater than 120 LET and total dose hard to greater than 1 Mrad (Si), operating across the full temperature range commonly specified for space applications.

ADVANTAGES

- OUM uses a reversible structural phase change.
- Small active storage medium.
- Simple manufacturing process.
- Simple planar device structure.
- Low voltage single supply.
- Reduced assembly and test costs.
- Highly scalable- performance improves with scaling.

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- Multistates are demonstrated.
- High temperature resistance.
- Easy integration with CMOS.
- It makes no effect on measured CMOS transistor parametric.
- Total dose response of the base technology is not affected.

CONCLUSION

Unlike conventional flash memory Ovonic unified memory can be randomly addressed. OUM cell can be written 10 trillion times when compared with conventional flash memory. The computers using OUM would not be subjected to critical data loss when the system hangs up or when power is abruptly lost as are present day computers using DRAM a/o SRAM. OUM requires fewer steps in an IC manufacturing process resulting in reduced cycle times, fewer defects, and greater manufacturing flexibility. These properties essentially make OUM an ideal commercial memory. Current commercial technologies do not satisfy the density, radiation tolerance, or endurance requirements for space applications. OUM technology offers great potential for low power operation and radiation tolerance, which assures its compatibility in space applications. OUM has direct applications in all products presently using solid state memory, including computers, cell phones, graphics-3D rendering, GPS, video conferencing, multi-media, Internet networking and interfacing, digital TV, telecom, PDA, digital voice recorders, modems, DVD, networking (ATM), Ethernet, and pagers. OUM offers a way to realize full system-on-a-chip capability through integrating unified memory, linear, and logic on the same silicon chip.

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ABSTRACT

Nowadays, digital memories are used in each and every fields of day-to-day life. Semiconductors form the fundamental building blocks of the modern electronic world providing the brains and the memory of products all around us from washing machines to super computers. But now we are entering an era of material limited scaling. Continuous scaling has required the introduction of new materials.

Current memory technologies have a lot of limitations. The new memory technologies have got all the good attributes for an ideal memory. Among them Ovonic Unified Memory (OUM) is the most promising one. OUM is a type of nonvolatile memory, which uses chalcogenide materials for storage of binary data. The term "chalcogen" refers to the Group VI elements of the periodic table. "Chalcogenide" refers to alloys containing at least one of these elements such as the alloy of germanium, antimony, and tellurium, which is used as the storage element in OUM. Electrical energy (heat) is used to convert the material between crystalline (conductive) and amorphous (resistive) phases and the resistive property of these phases is used to represent **0**s and **1**s.

To write data into the cell, the chalcogenide is heated past its melting point and then rapidly cooled to make it amorphous. To make it crystalline, it is heated to just below its melting point and held there for approximately 50ns, giving the atoms time to position themselves in their crystal locations. Once programmed, the memory state of the cell is determined by reading its resistance.

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